REMARKS

This application has been reviewed in light of the Office Action dated June 30, 2005.

Claims 1-20 are now presented for examination. Claims 1, 6 and 16 are independent. Favorable review is respectfully requested.

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yeh et al. (U.S. Pat. No. 6,319,807) in view of Chong et al. (U.S. Pat. No. 6,534,390). The applicants respectfully submit that independent claims 1, 6 and 16 are patentable over the art cited by the Examiner, for the following reasons.

The present invention, as defined in claim 1, is directed to a method for fabricating a semiconductor device having a gate structure on a substrate. This gate structure is adjacent to a dielectric material. In one step of the claimed method, a gate dielectric is formed on an exposed portion of the substrate. A metal layer is then formed overlying the gate dielectric. A silicide contact is subsequently formed in contact with a portion of the metal layer remaining in the gate region. These features of the invention are also recited in claim 6; claim 6 includes a step of forming a first metal layer overlying the first gate dielectric, a step of forming a second metal layer overlying the second gate dielectric, and a step of forming a silicide contact in contact with portions of the first metal layer and the second metal layer remaining in the gate region. In addition, claim 16 (directed to a semiconductor device having a gate structure on a substrate) recites a metal layer in contact with the gate dielectric, and a silicide contact which is in contact with the metal layer.

Yeh et al. is understood to disclose a method for forming an FET gate structure in which a dummy gate 240A, formed from a nitride layer, is removed and replaced with a polysilicon gate. In particular, Yeh et al. teaches forming reverse-offset nitride spacers 310 in the gate region, followed by formation of a gate oxide 315 (Figure 2J; col. 2, lines 57-63). A polysilicon gate 320 is then formed in contact with the gate oxide (Figure 2K; col. 2, line 65, to col. 4, line 2). Finally,

Yeh et al. teaches formation of a silicide contact ("Ti-saliciation," Figure 2K, col. 4, lines 3-6) on top of the polysilicon gate.

The applicants wish to point out that Yeh et al. does not disclose or suggest any metal layer overlying the gate dielectric, and thus cannot suggest any silicide contact which is in contact with that metal layer. The differences between the present invention and Yeh et al. may be easily seen by comparing Yeh et al. Figure 2K with Figure 5B of the specification. According to Yeh et al., a silicide contact 330 is in contact with polysilicon 320; in the present invention, silicide 51 is in contact with metal layer 26. It is noteworthy that Yeh et al. is primarily concerned with formation of a reverse-offset spacer (see col. 1, lines 8-10), and does not envision single-metal or dual-metal gates as in the present invention. Since Yeh et al. neither discloses nor suggests the above-noted features of the present invention, the present invention would not have been obvious therefrom.

Chong et al. is understood to disclose a semiconductor fabrication process in which a silicide contact is formed on top of a gate. In Chong et al. Figure 10, a silicide contact 36 overlies a polysilicon gate layer 16. Chong et al. refers to the gate as a "basic structure" (see col. 2, lines 21-34) and refers to the polysilicon gate 16 as "well known in the art" (col. 2, line 34). Chong et al. offers no teaching or suggestion regarding a metal gate, or any process for replacing a gate structure with a metal gate. Chong et al. clearly does not suggest a metal layer overlying a gate dielectric, or a silicide in contact with that metal layer, as in the present invention.

A combination of Yeh et al. and Chong et al. would at best yield a fabrication process in which a dummy gate is removed and replaced by a polysilicon gate with reverse-offset spacers, after which a silicide contact is formed using a laser annealing process. Neither of the references, nor a combination thereof, suggests any gate material other than polysilicon. Furthermore, neither reference, nor a combination thereof, suggests a silicide contact which is in contact with a metal layer in a gate region.

Accordingly, the present invention would not have been obvious from either of the two cited references, or from a combination thereof.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing remarks, the applicants respectfully request favorable reconsideration and early passage to issue of the present application.

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